A Network Modeling and Design Method for a 2–18-GHz Feedback Amplifier

ANTHONY M. PAVIO, JR., MEMBER, IEEE

Abstract—**An accurate network theory and modeling method, including feedback loop circuit parasitics and device limitations, is presented for the design of broad-band microwave feedback amplifiers. Discussed are circuit realization and measured performance in relation to VSWR, gain flatness, and stability of a 2–18-GHz three-stage amplifier.**

I. Introduction

THE APPLICATION of controlled feedback to improve the performance of solid-state and vacuum tube amplifiers is well known. However, as the upper frequency demands on wide-band MESFET amplifiers increase, accurate feedback design using classical techniques which employ ideal elements (R, L, C) becomes exceedingly difficult. The effects of FET mounting, bond wire lengths, and element parasitics, if not included in the design approach, degrade the validity of the resulting computed amplifier performance.

In this work a method to design multistage single-ended feedback amplifiers with extended high frequency performance is outlined. The design, analysis, and measured performance of several amplifiers as well as the application of this modeling method to monolithic circuit design are also discussed. Although the user requires some form of computer aided circuit analysis capability, due to the complex circuit modeling, he can quickly and easily analyze/optimize the desired amplifier using one of the Microwave CAD Programs currently available.

II. Amplifier Design Techniques

One of the prime areas of difficulty in designing cascaded MESFET amplifiers is controlling the impedance match between devices [1]. Shunt feedback can be used to reduce the magnitude of S_{11} and S_{22} at the terminals of the active elements, thus enabling the circuit designer to synthesize wide-band matching networks. Flat gain versus frequency and greatly improved amplifier stability, especially at lower microwave frequencies, are also desirable by-products of feedback [2],[3]. This improved circuit performance is not without cost; it is obtained at the expense of reduced transducer gain.

The simplified single-stage amplifier model shown in Fig. 1 can be analyzed using computer aided design methods to determine the approximate amount of RF feedback

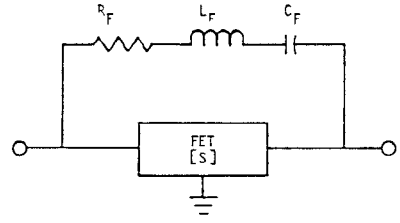


Fig. 1. Simplified feedback model.

that will produce the best compromise of the performance parameters. The effects of increasing shunt RF feedback on a typical FET is shown in Fig. 2. As the amount of feedback is increased (lower values of R_F) the magnitude of S_{11} and S_{22} are greatly reduced; however, this process cannot continue indefinitely since the maximum available gain of the device becomes too low to be of practical use. Even though S_{11} and S_{22} are not reduced to zero, the required transformation ratio of the matching networks is sufficiently reduced to allow for the easy design and realization of input/output and interstage networks [4]–[8]. In practice, when the feedback element values are lowered to reduce the FET maximum available gain, the gain versus frequency response begins to exhibit an upward slope. This effect is due to the fact that uniform amounts of negative feedback cannot be applied because of the finite phase shift of the feedback loop and the increasing phase shift as a function of frequency of the device. Hence, there will exist an optimum gain level obtainable with a particular FET and thin-film circuit.

As the operating frequency of the amplifier is increased, only small amounts of negative feedback can be tolerated since the open loop gain of the active device is becoming marginal. The natural gain rolloff of the FET is then compensated by reducing the amount of negative feedback at the upper frequency portion of the operating band. Typical values of S_{11}, S_{22}, and G_{MAX} are also shown in Fig. 2.

Based on the above analysis, a feedback loop is synthesized using ideal elements (R, L, C) and the resulting gain stage demonstrates a computed frequency response extending to 18 GHz. However, when the appropriate circuit parasitics, which are always present with any practical circuit realization are included, the high frequency performance of the amplifier is diminished. A circuit model for the true feedback loop including phase length and parasitics of the thin-film resistors, bond wire characteristics,

Manuscript received May 17, 1982; revised August 4, 1982. This work was supported in part by the Air Force Avionics Laboratory under Contract 33615-79-C-1919.

The author is with Texas Instruments Inc., Dallas, TX 75266.

0018-9480/82/1200-2212$00.75 ©1982 IEEE

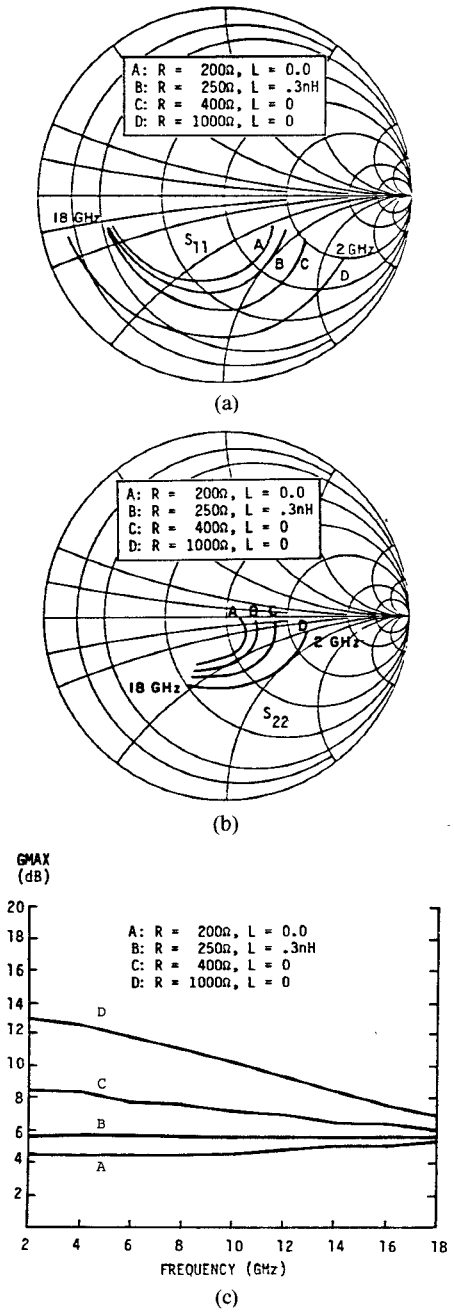


Fig. 2. (a) S_{11} as a function of R_F and L_F. (b) S_{22} as a function of R_F and L_F. (c) FET G_{MAX} (dB) as a function of R_F and L_F.

distributed inductance and capacitance effects will now be discussed.

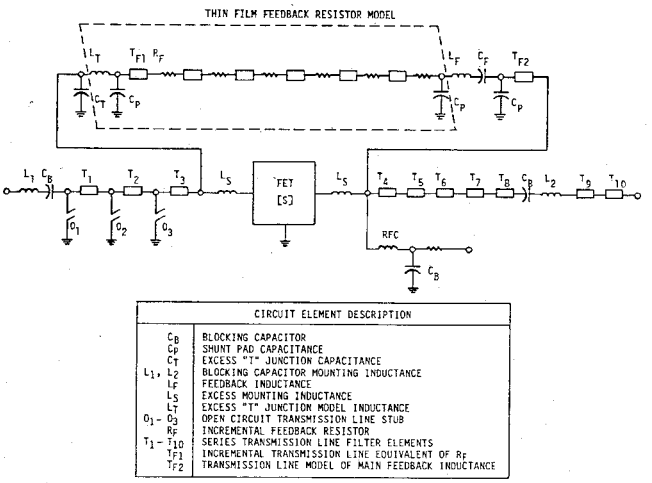
At frequencies above 14 GHz, the amplifier performance degradation due to these effects are pronounced. The active device mounting parasitics and phase transfer characteristics also greatly influence final circuit performance. To begin the model formulation, the FET must be characterized with the same mounting parasitics that will be present in the final amplifier. Thus, if self-biased amplifier operation is desired, S-parameter characterization should be performed with the correct values of source lead inductance and RF bypass capacitors. The input/output bond wire lengths which were used when the FET was mounted in the test fixture should be maintained in the final amplifier circuit. However, this is not an absolute requirement since small changes in the quantity of input or output series inductance can easily be accommodated; but, larger changes of inductance must be empirically determined.

An FET with high reverse isolation, low transducer phase shift, and a large transducer gain is essential in obtaining extended *Ku*-band performance. The total loop and transducer phase shift must be maintained such that large amounts of positive feedback do not occur. Although small amounts of positive feedback can improve the high frequency gain performance, large amounts of feedback can cause gain instability as a function of temperature as well as oscillation. Although small amounts of positive feedback can improve high frequency gain performance, the resulting amplifier will exhibit reduced gain versus temperature performance. This effect is especially evident in multistage designs where the changing output reflection coefficient (S_{22}) is accentuated by an interstage mismatching.

In order to minimize the phase shift encountered in the feedback loop, the resistor is deposited on the substrate using conventional thin-film methods and the surface area is kept as small as manufacturing constraints will permit. Although the feedback resistor is usually less than 0.005×0.010 in, the frequency response characteristics can be obtained from a ladder network model consisting of several resistor/transmission line sections. The most commonly used network consists of 6 sections, where $R_F = R_{FTOT}/N$ and $T_{F1} = Z_R(\Theta_S/N)$. The value of Z_R is the equivalent microstrip impedance corresponding to the feedback resistor width. The feedback inductance and resistor end pads are modeled as lossless transmission lines. A series/shunt model for the dc-blocking capacitor also includes its mounting effects. The parasitic effects associated with the resistor and blocking capacitor are minimized by constructing an amplifier on low dielectric substrates. Thus amplifiers realized on quartz substrates, although more difficult to fabricate than alumina designs, should exhibit superior high frequency performance.

Constrained computer aided optimization techniques are then used to restore the high frequency performance of the FET and modeled feedback loop [9]. The appropriate input and output or interstage network models can now be added to complete the amplifier design. The input and output networks added to the FET and feedback loop perturbate the calculated performance that was obtained with 50-Ω terminations. The loading effects of the matching networks and the effects on a nonzero S_{12} on the final amplifier performance are again eliminated by the use of network optimization. The resulting single-stage feedback amplifier model is shown in Fig. 3.

With a single-stage amplifier designed, multistage amplifiers can be constructed by cascading several gain stages. The reduced bandwidth and accentuated gain ripple resulting from directly cascading gain stages can be reduced or eliminated by adjusting the interstage networks (input/output network junctions) to obtain an amplifier



CIRCUIT ELEMENT DESCRIPTION	
C_B	BLOCKING CAPACITOR
C_P	SHUNT PAD CAPACITANCE
C_T	EXCESS "T" JUNCTION CAPACITANCE
L_1, L_2	BLOCKING CAPACITOR MOUNTING INDUCTANCE
L_F	FEEDBACK INDUCTANCE
L_S	EXCESS MOUNTING INDUCTANCE
L_T	EXCESS "T" JUNCTION MODEL INDUCTANCE
$O_1 - O_3$	OPEN CIRCUIT TRANSMISSION LINE STUB
R_F	INCREMENTAL FEEDBACK RESISTOR
$T_1 - T_{10}$	SERIES TRANSMISSION LINE FILTER ELEMENTS
T_{F1}	INCREMENTAL TRANSMISSION LINE EQUIVALENT OF R_F
T_{F2}	TRANSMISSION LINE MODEL OF MAIN FEEDBACK INDUCTANCE

Fig. 3. Single-stage feedback amplifier model.

with an equal ripple performance. It is not uncommon that the gain and bandwidth of a properly designed two-stage amplifier will usually compare favorably with the performance obtained with a single-stage design.

The parasitic elements which degrade the ultimate high frequency performance of feedback amplifiers can be reduced substantially with monolithic circuit implementations. The resistor lengths and the shunt capacitance associated with the mounting pad of the loop dc blocking capacitor can be made quite small. Sufficient capacitance can be obtained in an area of about 25-square mil. The phase shift of the overall loop can also be reduced because it can be placed closer to the active area of the device. By properly selecting the device size, the monolithic circuit designer can optimize the input VSWR and power output capabilities of the resulting amplifier.

III. Measured Performance

A variety of multistage amplifiers, constructed on various substrate materials have been designed. The 2–10-GHz two-stage amplifier shown in Fig. 4 was assembled on a 0.020-in-thick fused silica substrate. Nichrome thin-film resistors are used in the bias circuits and feedback network, and the required series inductance was realized with inductors wound with 0.001-in-diameter gold wire. These feedback loop elements are also clearly visable in Fig. 4. Fig. 5(a) depicts the two-stage amplifier's measured input/output VSWR and gain versus frequency response while the computed gain and return loss is shown in Fig. 5(b). A single-stage feedback amplifier was constructed on a fused silica substrate and the measured 2–10-GHz frequency response is shown in Fig. 6(a). It should be noted that the two-stage amplifier exhibits comparable bandwidth and gain ripple performance to the optimized single-stage design. The model of the FET that was used in the design of both amplifiers is shown in Fig. 6(b).

Since the input/output VSWR of the two-stage amplifier is low, several two-stage gain blocks can easily be cascaded without the need for balancing; thus, a reduction in amplifier size and number of devices needed for a particular gain requirement is achieved. By stagger tuning

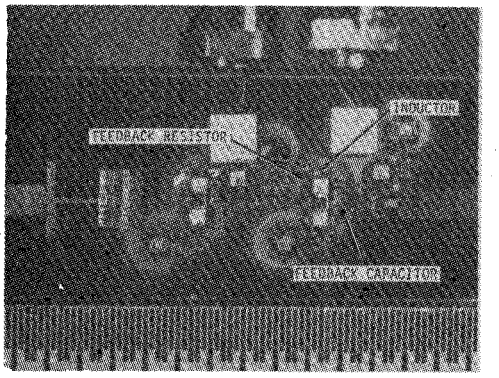


Fig. 4. Two-stage amplifier on quartz substrate.

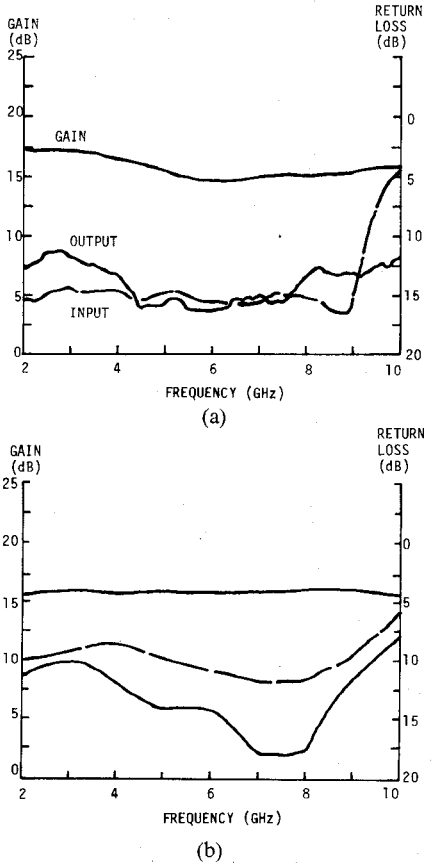


Fig. 5. (a) Measured performance of 2–10-GHz two-stage feedback amplifier. (b) Computed performance of 2–10-GHz two-stage feedback amplifier.

these amplifiers, the overall gain and bandwidth characteristics of the chain can be optimized.

The 2–18-GHz three-stage amplifier and its associated gain versus frequency response are shown in Figs. 7 and 8, respectively. This amplifier also displayed very uniform gain drift characteristics as a function of temperature, and the input/output reflection coefficients were virtually constant over the temperature range of $-55°C$ to $+85°C$. This outstanding temperature performance is primarily due to the reduction of the change, as a function of temperature, in S_{22} because of the use of RF feedback. Although no design constraints were imposed on the amplifier re-

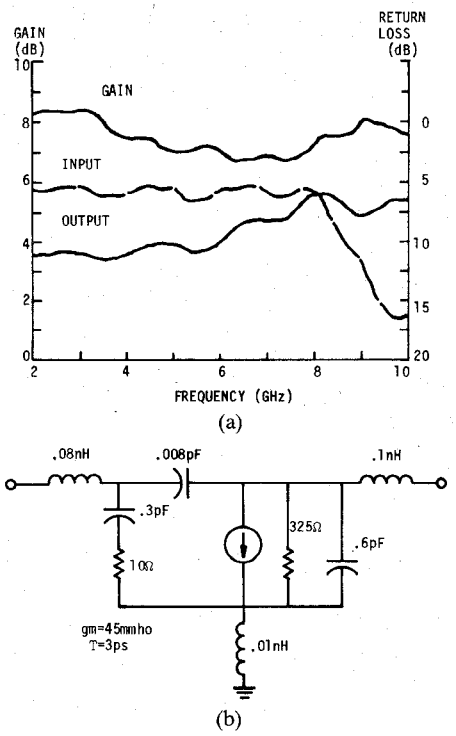


Fig. 6. (a) Single-stage amplifier performance. (b) FET model used in the design of the 2–10-GHz amplifier.

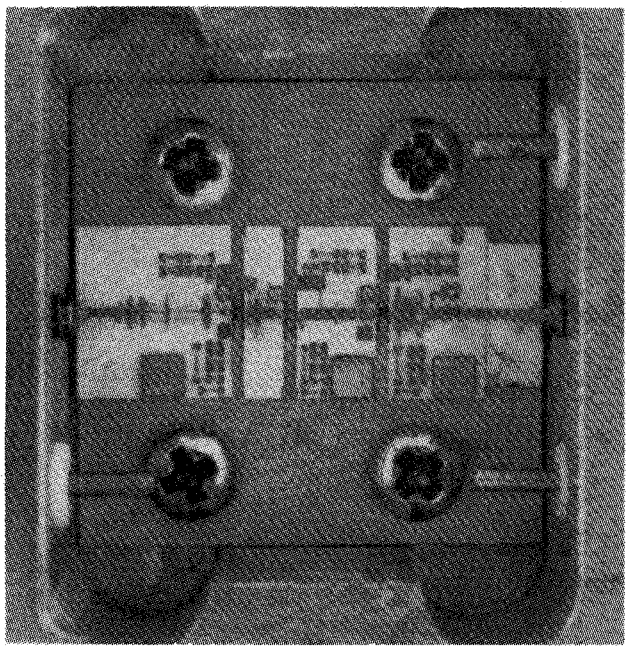


Fig. 7. Three-stage 2–18 GHz feedback amplifier.

garding noise figure performance, the measured noise figure in *Ku*-band was approximately 7 dB. A second amplifier which uses different FET's and self biasing, was assembled with the same thin-film networks. The gain versus frequency response of the amplifier is shown in Fig. 9. Fabrication of this amplifier was accomplished using thin-film circuit techniques on 0.010-in-thick alumina (Al_2O_3) substrates. Key to the amplifier's ability to perform at *Ku*-band frequencies is the minimization of the

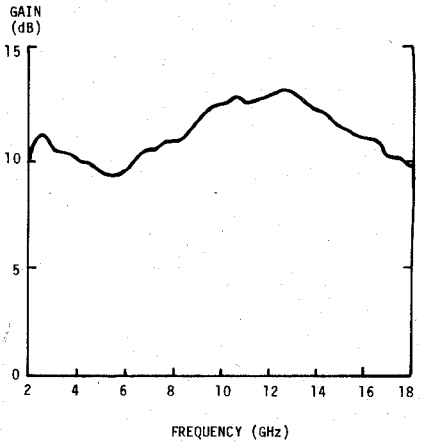


Fig. 8. Gain versus frequency response of 2–18-GHz three-stage feedback amplifier.

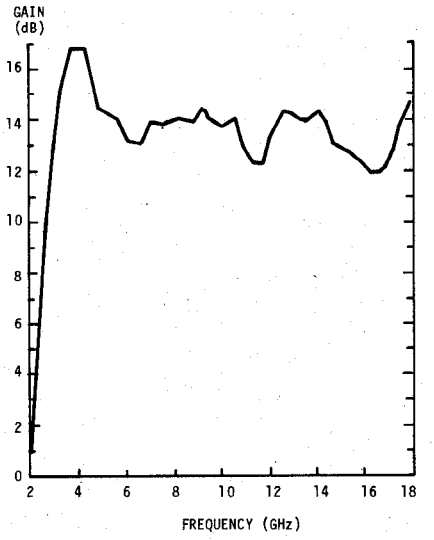


Fig. 9. Self-biased 2–18 GHz three-stage feedback amplifier gain versus frequency response.

effective phase length of the feedback loop and its associated parasitics by controlling the separation of the input, interstage, and output substrates and by using ultra small (0.010-in-square) dc-blocking capacitors.

IV. Conclusion

The illustrated design method enables the microwave engineer to easily synthesize and analyze broad-band feedback amplifiers with an added degree of confidence that the current simple circuit modeling techniques could not predict. The new circuit model and design philosophy are especially valuable at frequencies above 14 GHz. The excellent stability and impedance control characteristics allow amplifier gain chains to be constructed with cascaded multistage feedback gain blocks, certainly an important factor in reducing the cost, complexity, and size over conventional designs employing cascaded balanced hybrid coupled gain stages. Since these feedback techniques are applicable to monolithic circuits, accurate circuit modeling aids in the design of stable, single-ended amplifiers, where

costly design iterations and balanced configurations are neither desirable nor possible.

ACKNOWLEDGMENT

The author wishes to thank R. E. Jennings and R. E. Norton who aided in the assembly and tuning of the amplifiers.

REFERENCES

[1] E. Ulrich, "The use of negative feedback to slash wideband VSWR," *Microwaves*, Oct. 1978.
[2] K. B. Niclas, W. T. Wilser, R. B. Gold, and W. R. Hitchens, "The matched feedback amplifier ultra-wide-band microwave amplification with GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, Apr. 1980.
[3] _____, "A 350-MHz to 14-GHz MESFET amplifier using feedback," in *Dig. of Tech. Papers, Int. Solid-State Circuit Conf.*, Feb. 1980.
[4] G. L. Matthaei, "Short step Chebyshev impedance transformers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-14, Aug. 1966.
[5] G. L. Matthaei, "Tables of Chebyshev impedance transforming networks of low pass form," *Proc. IRE*, Aug. 1964.
[6] W. C. Petersen, "Analytical and computer aided design techniques for bipolar and FET transistor amplifiers," Ph.D. thesis, Cornell University, 1976.
[7] D. J. Mellor, "Computer aided synthesis of matching networks for microwave amplifiers," Ph.D. thesis, Stanford University, 1975.
[8] D. J. Mellor and J. G. Linvill, "Synthesis of interstage networks of prescribed gain versus frequency slopes," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, Dec. 1975.
[9] COMSAT General Integrated Systems, Inc., "Super Compact User Manual," 1981.

Anthony M. Pavio, Jr. was born in Waterbury, CT, in 1949. He received the B.S.E. and M.S.E.E. degrees in electrical engineering from the University of Connecticut in 1971 and 1972, respectively, and in 1982 received the Ph.D. degree in electrical engineering from Southern Methodist University.

From 1972 to 1974 he was employed as a Design Engineer at Raytheon Co. where his tasks included the design of broad-band stripline components, antennas, and power bi-polar amplifiers. During 1974 to 1979 he was employed at Rockwell International as a Senior Microwave Design Engineer where his duties included the RF design of communication satellite receivers. Dr. Pavio is currently employed at Texas Instruments where he is responsible for computer-aided microwave design and EW component development.

A Simplified "Real Frequency" Technique Applied to Broad-Band Multistage Microwave Amplifiers

BINBOGA SIDDIK YARMAN, MEMBER, IEEE, AND HERBERT J. CARLIN, FELLOW, IEEE

Abstract—**A computer-aided design (CAD) procedure, which is a new and simplified "real frequency" technique, is introduced for treating the broad-band matching of an arbitrary load to a complex generator. The method can be applied to the design of interstage equalizers for microwave amplifiers. It utilizes the measured data obtained from the generator and the load networks. Neither an *a priori* choice of an equalizer topology, nor an analytic form of the system transfer function, is assumed. The optimization process of the design procedure is carried out directly in terms of a physically realizable, unit normalized reflection coefficient which describes the equalizer alone.**

Based on the load-generator matching technique, a sequential procedure to design multistage microwave amplifiers is presented. An example is given for a three-stage, FET amplifier proceeding directly from the measured scattering parameters of the FET devices. The example is in three parts and illustrates the sequential method; that is, first a single-stage, then a two-stage, and finally the three-stage system is computed.

Manuscript received April 6, 1982; revised July 26, 1982. This work was supported in part by Joint Services Contract F49620-81-C-0082 and NSF Grant ECS811787875.

B. S. Yarman was with the School of Engineering, Cornell University, Ithaca, NY. He is presently with RCA, David Sarnoff Research Center, Princeton, NJ 08540.

H. Carlin is with the Department of Electrical Engineering, Cornell University, Ithaca, NY 14853.

I. INTRODUCTION

IN THE DESIGN of broad-band, multistage microwave amplifiers a fundamental problem is to realize lossless interstage equalizers as well as front-end and back-end equalizers so that the transfer of power from source to load is maximized over a prescribed frequency band. In such a case the problem is one of "double matching" power transfer from a complex generator to an arbitrary load (Fig. 1). In this paper, we will first introduce a new computer-aided design procedure, a simplified "real frequency" technique for double-matching problems, then we will extend the technique to the design of broad-band, multistage FET amplifiers.

0018-9480/82/1200-2216$00.75 ©1982 IEEE